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Two Stage PFC Boost Doubler with Interleaved Control Scheme

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Abstract: A diode bridge with two power switches is employed as a PFC circuit to achieve a high power factor and low line current harmonic distortion. Interleaved Control Scheme (ICS) scheme with PI voltage controller and PI current controller is used to generate three-level PWM on the dc side of diode rectifier. Based on the control scheme, the line current is driven to follow the sinusoidal current command which is in phase with the supply voltage, and the output voltage is found to be balanced. At rated power, the source current THD value is less than 5% when PI as voltage and current controller in the ICS.

Keywords: ICS, THD, HCC, PWM, PI, Power Factor, Total Harmonic Distortion (THD), Dual boost converter, Boost doubler

I. INTRODUCTION

Generally speaking, the PFC function includes shaping the current waveform and regulating the output voltage [1]. Due to the continuous input current, the boost-type converter has been widely integrated to the switch-mode rectifier (SMR) to achieve the desired PFC function [2]. The gate signal *GT* is obtained from the comparison of controller output signal v_{cs} and sawtooth signal. ICS includes an inner current loop and an outer voltage loop, and it is often used to generate the gate signal for the conventional boost-type SMR. One inductor current signal is fed back to the inner current loop to shape the current waveform. The output voltage is sensed for the outer voltage loop to regulate the output voltage. Sensing input voltage is also required for the generation of the desired current reference [3], [4] and the feedforward terms [5], [6]. In [7] and [8], some compensation loops are added to the multiloop control to improve the PFC performance for motor drive applications. For the boost converter, the single switch needs to withstand the overall output voltage when the switch blocks. The three-level boost converter is shown in Fig. 1 where two capacitors are connected across the switches, respectively. Thus, each switch needs to withstand only a half output voltage. In addition, the inductor voltage in the three-level boost converter has three levels, but the inductor voltage in the conventional boost converter has only two levels. Therefore, the three-level boost converter is able to yield smaller inductor current ripple than the conventional boost converter. It follows that three-level converters are often used in the applications, such as the high-voltage–ratio dc/dc conversion [9]–[12] and the wide input voltage range [13], particularly in the fuel cell applications [11], [13] and the grid-connected applications [10], [14], [15]. Additionally, the high-withstanding-voltage semiconductor switches often have larger drain–source resistances than the low-withstanding-voltage ones. Thus, the three-level converter has the advantages of low voltage stress, small inductor current ripple, and low switching loss [1], [11], [16].

II. MODELING OF AC-DC PFC BOOST DOUBLER

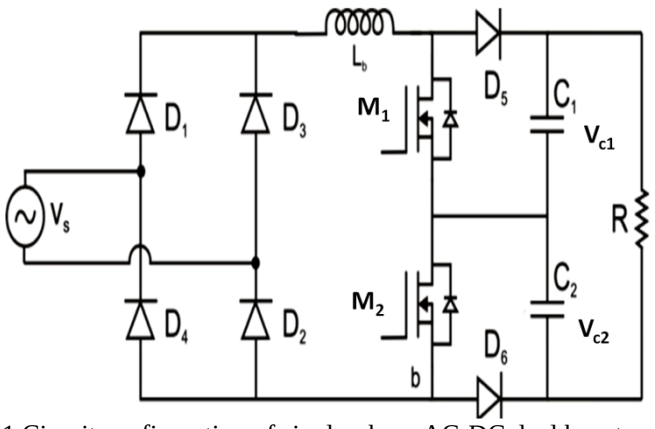

Fig. 1 Circuit configuration of single-phase AC-DC dual boost converter

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Fig 1 shows the single phase AC-DC dual boost converter. This circuit strategy consists of a single phase diode bridge rectifier, two power switching devices, one inductor, two fast recovery diodes and two dc capacitors. An inductor L_b is used to reduce current ripple. The voltage rating of the power semiconductors are reduced to half of dc bus voltage. The inductor boost volume is one quarter of the conventional boost converter. The single phase three level rectifier can be analysed in its four operating modes according to the states of two power semiconductor switches M_1 and M_2.

Table 1 Design value of circuit components

S.No	Parameter	Specification
1	Input line voltage (Vs)	28 V
2	Output voltage	48 V
3	Output power	100 W
4	Switching frequency (fs)	20 kHz
6	Line frequency	50 Hz
7	Boost inductor (Lb)	3 mH
8	Capacitance C1=C2	6000 µF
9	Load resistance	23 Ω

Table 1 shows the design values of circuit components used in two stage AC-DC dual boost converter.

A. Interleaved Control Scheme (ICS)

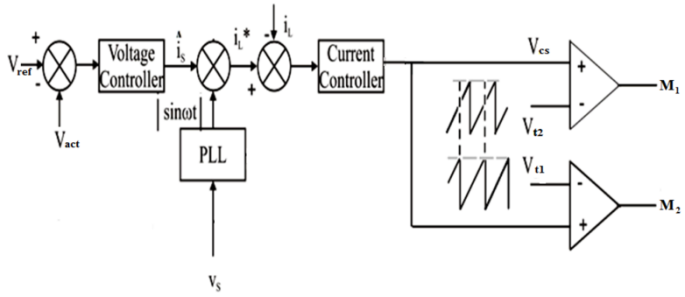

Fig. 2 Block diagram of *Interleaved Control Scheme (ICS)*

Fig 2 shows the Interleaved Control Scheme (ICS) block of the single phase AC-DC dual boost converter. It comprises of phase locked loop, conventional multi loop control with voltage controller and current controller, feed forward loop and interleaved PWM scheme. In outer voltage control loop, the converter output voltage is sensed and compared with the reference voltage. After comparison, error signal is fed to the voltage controller. The supply voltage is processed by the phase locked loop in order to produce absolute value of |sinωt|. The voltage controller output and absolute value of sinωt are used to obtain the amplitude of reference inductor current. This reference inductor current is compared with actual inductor current. After comparison, error signal is fed to the inner current control loop.

The comparator is used to compare the two ramp signals with the control signal generated, $V_{cs.}$ Two gate signals are generated from the comparisons between the control signal V_{cs} and two sawtooth signals V_{t1} and V_{t2}.

These two sawtooth signals have equal amplitude and identical period T_s but there is 180° phase difference between them. The comparator produces the pulses for switches M_1 and M_2 when the control signal is greater than the ramp signals.

B. Design of PI Controller

The PI controller takes into account the desired output of the converter to produce control signal which is necessary to reduce the error signal approximately to zero. A proportional controller gain (K_p) has the effect of reducing the rise time and does not eliminate the steady state error. An integral control gain (K_i) has the effect of eliminating the steady state error but makes the transient response worse. The error voltage obtained from the comparison of reference output voltage and actual output voltage is fed to the PI voltage controller in order to produce the peak value of input current.

An error signal, e(t) is used to control the switches in a converter. This error is the difference between the desired current, i_{ref}, and the current through the boost inductor, i_{act}. This error current is given to PI current controller. After processed by PI controller, The control signal v_{cs} is generated.

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III. SIMULATION OF THE SYSTEMS

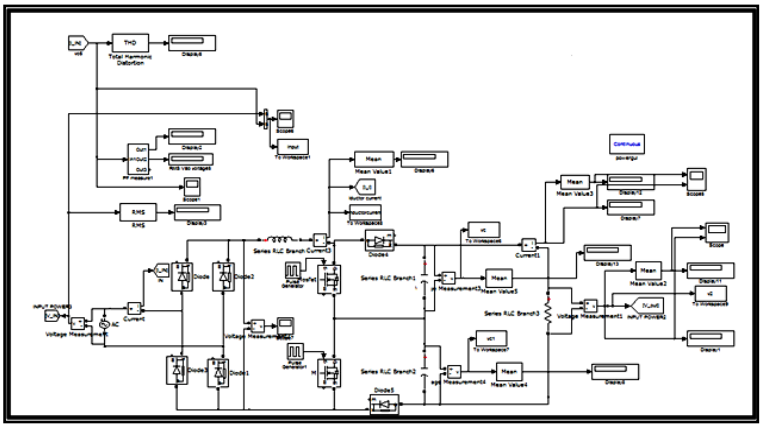

Fig. 3 Simulated circuit diagram of three level AC-DC converter with open loop control

Fig 3 shows the simulated circuit diagram of single phase AC-DC three level converter with open loop control.

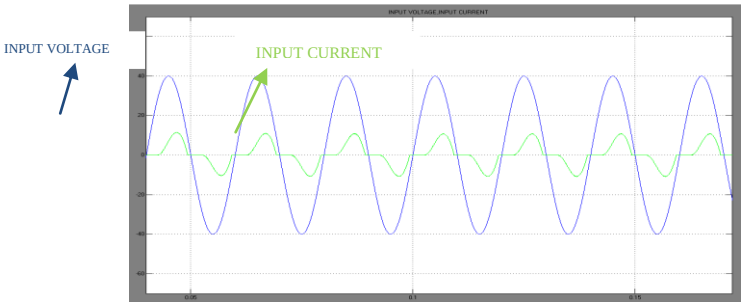

Fig. 4 Input voltage and input current waveform for open loop control

Fig 4 shows the input voltage and input current waveform with open loop control. This non sinusoidal input current is due to harmonic distortion in input current waveform.

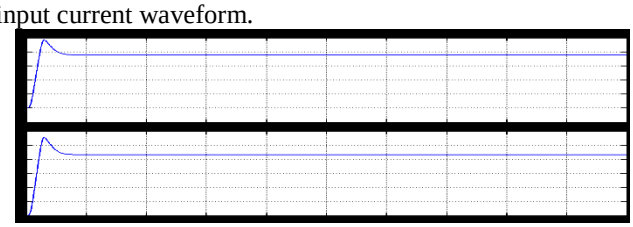

Fig. 5 Output current and output voltage waveform for open loop control

Fig 5 shows the output voltage and output current obtained from the open loop simulation of three level converter. The desired output voltage of 48V is not obtained in open loop control.

Table 2 Open loop analysis

Percentage of Load (%)	Output Voltage (V)	Input Current THD (%)	Power Factor
100	43.5	51.41	0.7777
75	44.94	56.75	0.7743
50	46.72	64.29	0.7652
25	49.17	77.17	0.7417

Table 2 shows the performance analysis of open loop control of single phase three level converter by varying the load resistance. for rated load, the total harmonic distortion of source current is very high and the value of THD obtained is 51.41%.

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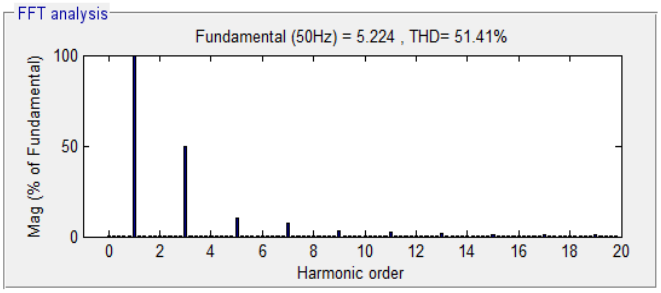

Fig. 6 FFT analysis for open loop control

Fig 6 shows the FFT analysis of total harmonic distortion with open loop control. By increasing load resistance, output voltage and THD are increased. But input power factor and efficiency are decreased. According to IEEE norms, harmonic should be less than 5%, which is not obtained in open loop control.

IV. CLOSED LOOP ANALYSIS

Closed loop control is a feedback control that deals with the behavior of dynamical systems with inputs. The external input of a system is called the reference. When one or more output variables of a system need to follow a certain reference over time, a controller manipulates the inputs to a system to obtain the desired effect on the output of the system.

C. Single phase three level AC-DC converter with PI voltage controller and PI current controller

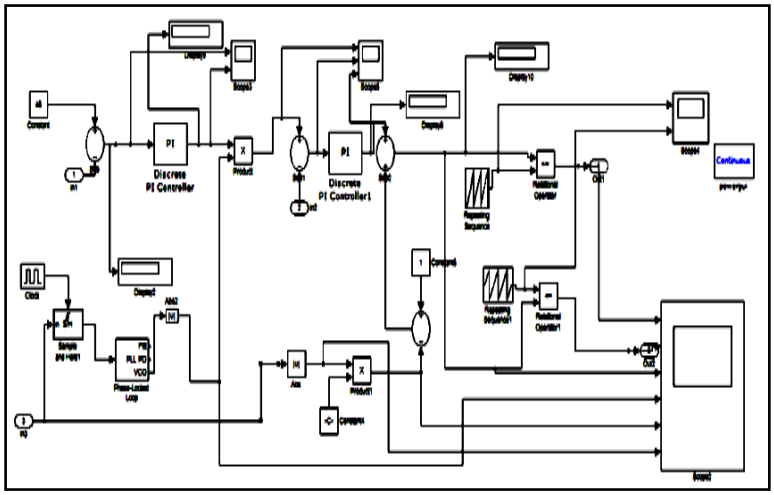

Fig. 7 Simulated circuit diagram of three level AC-DC converter with PI voltage controller and PI current controller

Fig 7 shows the simulated circuit diagram of proposed converter with PI controller. The proportional gain, integral gain values of PI controller is obtained from the transfer function of three level AC-DC converter with proper tuning. In PI control technique input current and output voltage are controlled by PI control.

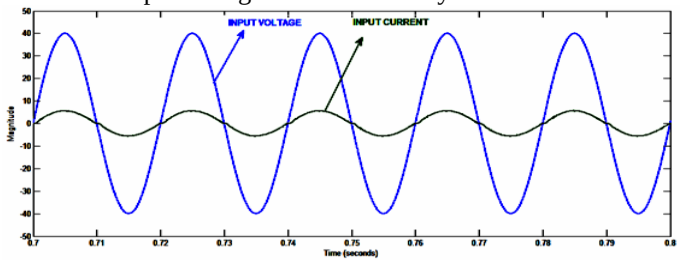

Fig. 8 Input voltage and input current waveforms for PI voltage controller and PI current controller

Fig 8 shows the input voltage and input current waveforms for proportional integral control. Input voltage and input current waveforms are in phase. Therefore input power factor is closed to unity. Input current waveform is slightly distorted.

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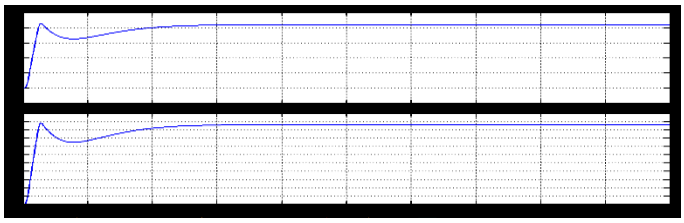

Fig. 9 Output current and output voltage waveforms for PI voltage controller and PI current controller

Fig 9 shows the output current and output voltage waveforms with PI voltage controller and PI current controller. From this waveform, the output voltage is maintained at 48V.

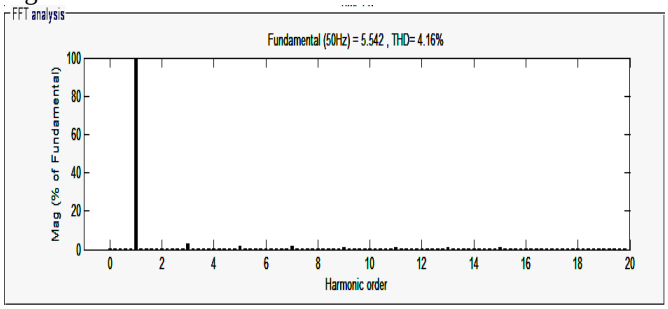

Fig. 10 FFT analysis for PI voltage controller and PI current controller

Fig 10 shows the FFT analysis of source current using PI voltage controller and PI current controller at rated load condition.

Table 3 Closed loop analysis

Percentage of Load (%)	Output Voltage (V)	Input Current THD (%)	Power Factor
100	48	4.16	0.9990
75	48	4.98	0.9986
50	48	5.82	0.9977
25	48	7.41	0.9963

Table 3 shows the performance analysis of boost doubler for variation in loads. At rated load condition, source current total harmonic distortion is 4.16%. The input power factor becomes 0.9990 (i.e) nearly unity. By increasing the load resistance, source current harmonics also increases and output voltage is maintained constant.

V. CONCLUSIONS

The Interleaved Control Scheme of single phase AC-DC PFC boost doubler was simulated with variation in load. It is noted that no voltage balancing loop, capacitor voltage sensing and feedforward loop are required in this proposed ICS. The simulation was done for the boost doubler with combinations of various controllers such as PI voltage controller and PI current controller. PI controller integrated ICS reduces the THD value to 4.16% without adding any filter on supply side and power factor closer to unity.

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